REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated November 16, 2005. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due consideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 23-28 are under consideration in this application. Claims 23 and 27-28 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicant's invention.

The claims are being amended to correct formal errors and/or to better recite or describe the features of the present invention as claimed. All the amendments to the claims are supported by the specification. Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

Allowable Subject Matter

Claim 27 would be allowed if rewritten in independent form to include all limitation of the base claim and intervening claims.

As claim 27 is being rewritten in independent form to include all limitation of the base claim and intervening claims, it is in condition for allowance.

Prior Art Rejections

Claims 23-26 and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 5,059,899 to Farnworth et al. (hereinafter "Farnworth") in view of US Patent No. 5,760,643 to Whelsel (hereinafter "Whelsel"). The prior art references of Jassowski (5,641,978), Morris (6,433,628), and Shimanuki et al. (6,930,380) were cited as being pertinent to the present application. The above rejection has been carefully considered, but is most respectfully traversed.

The semiconductor integrated circuit device of the invention (for example, the embodiment depicted in Fig. 1), as now recited in claim 23, comprises: a semiconductor chip 1 embedded in the semiconductor integrated circuit device. The semiconductor chip 1

comprising: a first bonding pad arranged on a first side (e.g., the upper side) of the semiconductor chip 1; a second bonding pad 311 arranged on a second side (e.g., the left side) of the semiconductor chip; a first input and output buffer 4 and a second input and output buffer which are coupled to the first and second bonding pads respectively; a first inspection pad 211; a first connecting wire 411 which is laid outside an area where the first and second input and output buffers are arranged and which connects the second bonding pad 311 to the first inspection pad 211. The first inspection pad 211 is arranged on the first/upper side of the semiconductor chip and only connected to one bonding pad on the second/left side of the semiconductor chip (Fig. 1; p. 11, line 10 to p. 12, line 4) such that the second bonding pad 311 on the second/left side and the first bonding pad on the first/upper side are set to be tested concurrently through respectively probing the first inspection pad 211 and the first bonding pad on the first/upper side (p. 12, lines 5-12).

As the first inspection pad 211 (wired with the second bonding pad 311) is arranged on the first/same side of the chip as the first bonding pad, the first and second bonding pads can be probed simultaneously with probes lined in one direction on the first side, despite the first and second bonding pads being arranged on different sides of the chip. Accordingly, the invention probes the chips quickly without using probe cards of special shapes (P. 5, lines 4-14) and reduces the cost in manufacturing the chips.

Applicants respectfully contend none of the cited references teaches or suggests "that the first inspection pad 211 is arranged on the first/upper side of the semiconductor chip and only connected to one bonding pad on the second/left side of the semiconductor chip such that the second bonding pad 311 on the second/left side and the first bonding pad on the first/upper side are tested concurrently through respectively contacting the first inspection pad 211 and the first bonding pad on the first/upper side" as the invention.

In contrast, Farnsworth's interface test pad 20/36 is arranged in the scribe area (col. 2, lines 46-47; col. 3, lines 51-52) outside of the semiconductor chip 12/30, rather than comprised inside of the semiconductor chip as the first inspection pad 211 "arranged on the first/upper side of the semiconductor chip" of the invention.

In addition, Farnsworth's interface test pad 20/36 is connected to **four/two** bonding pads 18/34 in four/two different semiconductor chips 12/30 (Figs. 2-3), rather than being only connected to **one** bonding pad on the second/left side of the same semiconductor chip 1, as in the invention.

Farnsworth further does not show a semiconductor chip having a bonding pad and an inspection pad (which is wired with another bonding pad on another side) arranged on the same side of the semiconductor chip "such that the second bonding pad 311 on the second/left side and the first bonding pad on the first/upper side are set to be tested concurrently through respectively probing the first inspection pad 211 and the first bonding pad on the first/upper side" as the invention. Thus, Farnsworth cannot simultaneously probe bonding pads arranged on four sides (upper, lower, right, and left) of the same chip with probes 8 aligned only on two sides (upper and lower) so as to increase the probing speed and reduce the probing cost as does the invention (Fig. 2).

Applicants contend that Farnworth fails to teach or disclose each and every feature of the present invention as disclosed in independent claim 23. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, Applicants respectfully submit that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the

prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and telephone number indicated below.

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